IN THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

1-5. (Canceled)

6. (**Currently Amended**) An apparatus comprising a machine-readable medium containing instructions which, when executed by a machine, cause the machine to perform operations comprising:

assigning a first register class to at least one symbolic register in at least one instruction;

assigning a second register class to the at least one symbolic register through conjunctive forward dataflow analysis;

~~reducing~~ **moving** register class fixups for the assignment of the second register class **and removing unnecessary register class fixups to reduce the register class fixups**; and

renaming the at least one symbolic register,

wherein each instruction includes assignment of one of the first register class assigned and the second register class assigned.

7. (Original) The apparatus of claim 6, said assigning the first register class instruction is an initial assignment.

8. (Previously Presented) The apparatus of claim 6, said assigning the second register class further including instructions which, when executed by a machine, cause the machine to perform operations including:

marking a register class assignment map that operates to track register class assignments at a block entry of a compilation unit;

marking the register class assignment map at a block exit of the compilation unit;

determining the register class assignment map at an entry of a instruction in a block; and

determining the register class assignment map at an exit of a instruction in the block.

9. (**Currently Amended**) The apparatus of claim 6, said ~~reducing~~ **moving** register class fixups ~~further including instructions which, when executed by a machine, cause the machine to perform operations including:~~ **comprises one or more of** hoisting register class fixups[[;]] **and** sinking the register class fixups~~; and removing the register class fixups that are unnecessary~~.

10. (**Currently Amended**) The apparatus of claim [[9]] **6**, **wherein** said removing the register class fixups that are unnecessary ~~further including instructions which, when executed by a machine, cause the machine to perform operations including~~ **comprises** removing dead code.

11. (**Currently Amended**) A system comprising:

a processor having at least one register; and

a compiler coupled to the processor executing in a host device that inputs a source program having a plurality of operation blocks,

wherein the compiler assigns a first register class in at least one instruction to the at least one symbolic register, and assigns a second register class through conjunctive forward dataflow analysis to the at least one symbolic register, ~~reduces~~ **moves** register class fixups for the assignment of the second register class **and removes unnecessary register class fixups to reduce the register class fixups**, and renames the at least one symbolic register,

wherein each instruction includes assignment of one of the first register class assigned and the second register class assigned.

12. (Original) The system of claim 11, wherein the first register class assigned is an initially assigned register class.

13. (Previously Presented) The system of claim 11, wherein the second register class assigned includes:

marking a register class assignment map that operates to track register class assignments at a block entry of a compilation unit;

marking the register class assignment map at a block exit of the compilation unit;

determining the register class assignment map at an entry of a instruction in a block; and

determining the register class assignment map at an exit of a instruction in the block.

14. (**Currently Amended**) The system of claim 11, said ~~reduction~~ **movement** of register class fixups includes **one or more of**:

hoisting register class fixups; **and**

sinking the register class fixups~~; and~~

~~removing the register class fixups that are unnecessary~~.

15. (**Currently Amended**) The system of claim [[14]] **11**, said removing the register class fixups that are unnecessary includes removing dead code.

16. (**Currently Amended**) A computer comprising:

at least one processor having at least one register coupled to a first memory and a second memory;

at least one user input device coupled to the processor;

a monitor coupled to the processor, and

a compiler executing in the processor that inputs a source program having a plurality of operation blocks,

wherein the compiler assigns a first register class in at least one instruction to the at least one register, assigns a second register class through conjunctive forward dataflow analysis to the at least one register, ~~reduces~~ **moves** register class fixups for the assignment of the second register class **and removes unnecessary register class fixups to reduce the register class fixups**, and renames the at least one register,

wherein each instruction includes assignment of one of the first register class assigned and the second register class assigned.

17. (Original) The computer of claim 16, wherein the first register class assigned is an initially assigned register class.

18. (Previously Presented) The computer of claim 16, wherein the second register class assigned includes:

marking a register class assignment map that operates to track register class assignments at a block entry of a compilation unit;

marking the register class assignment map at a block exit of the compilation unit;

determining the register class assignment map at an entry of a instruction in a block; and

determining the register class assignment map at an exit of a instruction in the block.

19. (**Currently Amended**) The computer of claim 16, said ~~reduction~~ **movement** of register class fixups includes **one or more of**:

hoisting register class fixups; **and**

sinking the register class fixups~~; and~~

~~removing the register class fixups that are unnecessary~~.

20. (**Currently Amended**) The computer of claim [[19]] **16**, **wherein** said removing the register class fixups that are unnecessary includes removing dead code.